

a second pMOS transistor;

a third pMOS transistor having a gate coupled to the inverse input of the amplifier and having a source coupled to a source of the first pMOS transistor and to a drain of the second pMOS transistor;

a first nMOS transistor having a gate coupled to the input of the amplifier;

a second nMOS transistor having a gate coupled to a drain of the first pMOS transistor, a drain of the first nMOS transistor, and to a gate of the second pMOS transistor; and

a third nMOS transistor having a gate coupled to the inverse input of the amplifier, a drain coupled to a drain of the third pMOS transistor and a source coupled to a source of the first nMOS transistor and to a drain of the second nMOS transistor, wherein the output of the amplifier is coupled to the drain of the third pMOS transistor and to the drain of the third nMOS transistor.

58. (New) The apparatus as claimed in claim 57, the amplifier further comprising a resistor, wherein the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled directly together, and the drain of the first pMOS transistor and the drain of the first nMOS transistor are coupled directly together, wherein the direct coupling of the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled via the resistor to the direct coupling of the drain of the first pMOS transistor and the drain of the first nMOS transistor.

59. (New) The apparatus according to claim 58, wherein the resistor has a resistance of approximately 5000 ohms.

60. (New) The apparatus according to claim 57, the amplifier further comprising a control input, wherein the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled to the control input.

61. (New) The apparatus according to claim 57, wherein a width of each of the first pMOS transistor, the second pMOS transistor and the third pMOS transistor is approximately 9.2um, and wherein a width of the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 4um.

62. (New) The apparatus according to claim 61, wherein a length of each of the first pMOS transistor, the second pMOS transistor, the third pMOS transistor, the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 80nm.

63. (New) The apparatus as claimed in claim 16, the amplifier further comprising:

an input;

an inverse input;

a first pMOS transistor having a gate coupled to the input of the amplifier;

a second pMOS transistor;

a third pMOS transistor having a gate coupled to the inverse input of the amplifier and having a source coupled to a source of the first pMOS transistor and to a drain of the second pMOS transistor;

a first nMOS transistor having a gate coupled to the input of the amplifier;

a second nMOS transistor having a gate coupled to a drain of the first pMOS transistor, a drain of the first nMOS transistor, and to a gate of the second pMOS transistor; and

a third nMOS transistor having a gate coupled to the inverse input of the amplifier, a drain coupled to a drain of the third pMOS transistor and a source coupled to a source of the first nMOS transistor and to a drain of the second nMOS transistor, wherein the output of the amplifier is coupled to the drain of the third pMOS transistor and to the drain of the third nMOS transistor.

64. (New) The apparatus as claimed in claim 63, the amplifier further comprising a resistor, wherein the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled directly together, and the drain of the first pMOS transistor and the drain of the first nMOS transistor are coupled directly together, wherein the direct coupling of the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled via the resistor to the direct coupling of the drain of the first pMOS transistor and the drain of the first nMOS transistor.

65. (New) The apparatus according to claim 64, wherein the resistor has a resistance of approximately 5000 ohms.
66. (New) The apparatus according to claim 63, the amplifier further comprising a control input, wherein the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled to the control input.
67. (New) The apparatus according to claim 63, wherein a width of each of the first pMOS transistor, the second pMOS transistor and the third pMOS transistor is approximately 9.2um, and wherein a width of the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 4um.
68. (New) The apparatus according to claim 67, wherein a length of each of the first pMOS transistor, the second pMOS transistor, the third pMOS transistor, the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 80nm.